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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,474	12/01/2003	Masood Murtuza	TI-35639	5891

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
10/12/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/726,474	MURTUZA, MASOOD	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8,10,12-14 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10,12-14 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 08/08/2007 has been entered.

Response to Arguments

2. Applicant's arguments filed 08/08/2007 have been fully considered.

It is argued, at page 5 of the remarks, that "Davis also teaches a dielectric layer 73 [that] does not satisfy the claimed additional ILD layer because a contact layer [37-38] does not overly dielectric layer 73 and dielectric layer 73 does not isolate the contact layer from the support structures. As discussed in paragraph 33 of Davis, metal lines 37-38 and metal pads 45 are formed out of the final metal layer 71 (located below dielectric layer 73 rather than over it). In Davis, the support structures 47 are connected to the final metal layer 71 rather than isolated from it by an additional ILD layer as claimed. Davis does not disclose or suggest a contact."

There is certainly no difference between the isolation provided to Davis' bond pads 47 (formed from contact layer 37-38, as seen in Davis' figure 4) and the isolation of Applicant's bond pads 222, as seen in Applicant's figures 11-12. Further, in figures 2-4 Davis clearly shows layers 37-38 formed over the entire support structure, including (presumably) dielectric layer 73.

However, Davis presents a troubling ambiguity, as Applicant points out. In paragraph 0033 Davis states that layers 37-38 are formed from layer 71, clearly seen (in figure 5) as formed under (not over) dielectric layer 73.

In order to err on the side of caution Applicant's arguments must be considered persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection have been made in view of Lin, and in view of Ghoshal. This action is non-final as a consequence

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-5,7,8,10,12-14 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by LIN (2004/0253801).

With regard to claims 1-5,7, 8, and 10, Lin discloses a semiconductor device comprising a substrate 50; a plurality of inter-level dielectric layers (ILD layers 30,32,60,64) each having an ultra-low dielectric constant (k); at least one support structure 30 (elsewhere recited as "a plurality of support structures"), being a via or trench (note paragraph 0070) formed from an tungsten support material disposed in each of the ILD layers 30,32,60,64 at locations overlying each other so that support structures 30 overly each other in the plurality of ILD layers 30,32,60,64; at least one additional ILD layer 24 having a dielectric constant which is higher than the low-k ILD layers 30,32,60,64 overlying the low-k inter-level dielectric layers; and a contact layer forming bond pad 18 overlying the at least one additional ILD layer 24 and the support structures 30, wherein the at least one additional ILD layer 24 isolates the contact layer 18 from the support structures 30, the support structures 30 being located underneath the bond pad 18 location and the support structure 30 ending at the at least one additional ILD layer 24. Note figures 1,6,7, and paragraphs 0062-0077 of Lin.

The applicant's claims 1-5,7, 8, and 10 do not distinguish over the Lin reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of the support structures being capable of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being

particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device; said bond pad location being capable of functioning as a source of stress.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property

which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007). Applicant will please note that the

fact one could reasonably expect the prior art to perform the recited function was enough to support a prima facie finding that the device claimed by virtue of the recital of said function was identical to (or obvious in view of, as the case may be) the prior art device.

In this case it is reasonable to assume that Lin's support structures are capable of the claimed functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device; said bond pad location being capable of functioning as a source of stress, because a comparison of Applicant's specification to Lin's disclosure reveals that Lin discloses a device having support structures that are apparently identical to the support structures Applicant describes as being capable of performing the functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device. Lin's bond pad location reasonably appears capable of functioning as a source of stress for the same reason.

Because it is reasonable to assume that assume that Lin's device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

With regard to claims 12 and 13, Lin discloses a semiconductor device comprising a substrate 50; a plurality of inter-level dielectric layers (ILD layers 30,32,60,64) each having a low dielectric constant (k); at least one support structure 30 disposed in each of the ILD layers 30,32,60,64 at locations overlying each other so that support structures 30 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 30,32,60,64; at least one additional ILD layer 24 having a dielectric constant which is higher than the low-k ILD layers 30,32,60,64 overlying the low-k inter-level dielectric layers; and a contact layer 18 overlying the at least one additional ILD layer 24 and the support structures 30, wherein the at least one additional ILD layer 24 isolates the contact layer 18 from the support structures 30; wherein a plurality of support structures 30 are disposed in at least one of the low-k dielectric layers in an n x m matrix configuration, where n and m are integers greater than one; and wherein the plurality of support structures 30 are disposed at a location below a bond pad 18 disposed on the semiconductor device, wherein the support structures 30 are disposed in the at least one low-k dielectric layer at a plurality of

locations spaced equidistant apart from each other across substantially the entire layer. Note figures 1,6,7, and paragraphs 0062-0077 of Lin.

24. With regard to claim 24, Lin discloses a semiconductor device comprising a substrate 50; a plurality of inter-level dielectric layers (ILD layers 30,32,60,64) each having a low dielectric constant (k); at least one support structure 30 disposed in each of the ILD layers 30,32,60,64 at locations overlying each other so that support structures 30 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 30,32,60,64; at least one additional ILD layer 24 having a dielectric constant which is higher than the low-k ILD layers 30,32,60,64 overlying the low-k inter-level dielectric layers; and a bond pad 18 overlying the at least one additional ILD layer 24 and the support structures 30. Note figures 1,6,7, and paragraphs 0062-0077 of Lin.

The applicant's claim 24 does not distinguish over the Lin reference regardless of the function allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the support structures being capable of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied. See *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ

136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]"), cited above. Applicant will please again note that the fact one could reasonably expect the prior art to perform the recited function was enough to support a prima facie finding that the device claimed by virtue of the recital of said function was identical to (or obvious in view of, as the case may be) the prior art device.

In this case it is reasonable to assume that Lin's support structures are capable of the claimed function of mitigating damage of the semiconductor device caused by stresses to the ILD layers, because a comparison of Applicant's specification to Lin's disclosure reveals that Lin discloses a device having support structures that are

apparently identical to the support structures Applicant describes as being capable of performing the function of mitigating damage of the semiconductor device caused by stresses to the ILD layers.

Because it is reasonable to assume that assume that Lin's device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

B. Lin may be overcome by appropriate Rule 131 affidavit by Applicant. Therefore, in the interest of compact prosecution claims 1-5,7,8,10,12-14 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ghoshal (6,204,165).

With regard to claims 1-5,7, 8, and 10, Ghoshal discloses a semiconductor device comprising a substrate 100; a plurality of inter-level dielectric layers (ILD layers 111,113,115,117,119,121) each having an ultra-low dielectric constant (k);

at least one support structure 190-171, (elsewhere recited as "a plurality of support structures 190-171") being a via (note column 1 lines 23-26) formed from an aluminum or copper support material disposed in each of the ILD layers 111,113,115,117,119,121 at locations overlying each other so that support structures 190-171 overly each other in the plurality of ILD layers 111,113,115,117,119,121;

at least one additional ILD layer 143 having a dielectric constant which is higher than the low-k ILD layers 111,113,115,117,119,121 overlying the low-k inter-level dielectric layers; and

a contact layer forming bond pad 190 overlying the at least one additional ILD layer 143 and the support structures 190-171, wherein the at least one additional ILD layer 143 isolates the contact layer 190 from the support structures 190-171, the support structures 190-171 being located underneath the bond pad 190 location and the support structure 190-171 ending at the at least one additional ILD layer 143. Note figure 1, column 2 lines 52-67, and column 3 lines 1-19 and 34-48 of Ghoshal.

The applicant's claims 1-5,7, 8, and 10 do not distinguish over the Ghoshal reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of the support structures being capable of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device; said bond pad location being capable of functioning as a source of stress.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]), makes it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") and *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable). See MPEP § 2114.

In *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), the Board found, "There is nothing in the Specification to indicate that the [property]

necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]." The Board held, "We thus agree with the Examiner that a prima facie case of anticipation is established by [the prior art]. Because the Appellant presented no evidence to overcome the Examiner's finding of the inherent ability of [the prior art's] [structure] to [perform the clamed function], she failed to meet her burden to overcome that prima facie case. We therefore find that claim 35 is anticipated by [the prior art]." The Board cited *In re King* for the proposition that "[A] prima facie case of anticipation [may be] based on inherency," and *In re Best* for the proposition that "Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product," in support if its holding. See *Ex parte* Smith, 83 USPQ2d 1509,1514 (Bd. Pat. App. & Int. 2007). Applicant will please note that the fact one could reasonably expect the prior art to perform the recited function was enough to support a prima facie finding that the device claimed by virtue of the recital of said function was identical to (or obvious in view of, as the case may be) the prior art device.

In this case it is reasonable to assume that Ghoshal's support structures are capable of the claimed functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device; said bond pad location being capable of functioning as a source of stress, because a comparison of Applicant's specification to Ghoshal's disclosure reveals that Ghoshal discloses a device having support structures that are apparently identical to the support structures Applicant describes as being capable of performing the functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied; the support structure being particularly capable of mitigating damage of the ILD layer in the event that forces might be applied onto the ILD layer during subsequent processing and packaging of the semiconductor device. Ghoshal's bond pad location reasonably appears capable of functioning as a source of stress for the same reason.

Because it is reasonable to assume that assume that Ghoshal's device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

With regard to claims 12 and 13, Ghoshal discloses a semiconductor device comprising a substrate 100; a plurality of inter-level dielectric layers (ILD layers 111,113,115,117,119,121) each having a low dielectric constant (k); at least one support structure 190-171 disposed in each of the ILD layers 111,113,115,117,119,121 at locations overlying each other so that support structures 190-171 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 111,113,115,117,119,121; at least one additional ILD layer 143 having a dielectric constant which is higher than the low-k ILD layers 111,113,115,117,119,121 overlying the low-k inter-level dielectric layers; and a contact layer 190 overlying the at least one additional ILD layer 143 and the support structures 190-171, wherein the at least one additional ILD layer 143 isolates the contact layer 190 from the support structures 190-171; wherein a plurality of support structures 190-171 are disposed in at least one of the low-k dielectric layers in an n x m matrix configuration, where n and m are integers greater than one; and wherein the plurality of support structures 190-171 are disposed at a location below a bond pad 190 disposed on the semiconductor device, wherein the support structures 190-171 are disposed in the at least one low-k dielectric layer at a plurality of locations spaced equidistant apart from each other across substantially the entire layer. Note figure 1, column 2 lines 52-67, and column 3 lines 1-19 and 34-48 of Ghoshal.

24. With regard to claim 24, Ghoshal discloses a semiconductor device comprising a substrate 100; a plurality of inter-level dielectric layers (ILD layers 111,113,115,117,119,121) each having a low dielectric constant (k); at least one support structure 190-171 disposed in each of the ILD layers 111,113,115,117,119,121 at locations overlying each other so that support structures 190-171 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 111,113,115,117,119,121; at least one additional ILD layer 143 having a dielectric constant which is higher than the low-k ILD layers 111,113,115,117,119,121 overlying the low-k inter-level dielectric layers; and a bond pad 190 overlying the at least one additional ILD layer 143 and the support structures 190-171. Note figure 1, column 2 lines 52-67, and column 3 lines 1-19 and 34-48 of Ghoshal.

The applicant's claim 24 does not distinguish over the Ghoshal reference regardless of the function allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the support structures being capable of mitigating damage of the semiconductor device caused by stresses to the ILD layers, if such stresses should ever be applied. See *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art]

does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); and *Ex parte* Smith, 83 USPQ2d 1509 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("There is nothing in the Specification to indicate that the [property] necessary to render the [claimed structure] [capable of the clamed function] is anything more than the inherent result of constructing the [claimed structure] of standard materials in accordance with claim 35's other limitations, which are expressly disclosed in [the prior art]"), cited above. Applicant will please again note that the fact one could reasonably expect the prior art to perform the recited function was enough to support a prima facie finding that the device claimed by virtue of the recital of said function was identical to (or obvious in view of, as the case may be) the prior art device.

In this case it is reasonable to assume that Ghoshal's support structures are capable of the claimed function of mitigating damage of the semiconductor device caused by stresses to the ILD layers, because a comparison of Applicant's specification to Ghoshal's disclosure reveals that Ghoshal discloses a device having support structures that are apparently identical to the support structures Applicant describes as being

capable of performing the function of mitigating damage of the semiconductor device caused by stresses to the ILD layers.

Because it is reasonable to assume that assume that Ghoshal's device is capable of performing the claimed function, the burden shifts to Applicants to show that it are not. See MPEP § 2114.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826